Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**SOURCE**

**GATE**

**.126”**

**.146”**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: S = .020” X .047” G = .030” X .036”**

**Backside Potential: DRAIN**

**Geometry: 574354**

**APPROVED BY: DK DIE SIZE .126” X .146” DATE: 4/13/18**

**MFG: SILICONIX THICKNESS .010” P/N: IRFC430**

**DG 10.1.2**

#### Rev B, 7/19/02